



Multiplexer/Decoder Implementation of Logic Functions

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EECS: 1100 Digital Logic Design
The University of Toledo

Lab Assignment #7

1. Objectives

- practicing the implementation of logic functions using MSI level functional blocks,
- gaining experience with MSI level functional blocks/components whose outputs are *active low*,
- practicing the consideration of alternate forms of expressions of logic functions in order to find a simpler logic circuit implementation,
- practicing the implementation of multiple input AND and OR functions using degenerate two-level logic circuit forms,
- gaining a close insight into the functioning and properties of decoder circuits,
- gaining a close insight into the functioning and properties of multiplexer (MUX) circuits,
- developing skills in the design and testing of combinational logic circuits.

2. Prelab Assignment

Algebraic form of a logic function $f(D,C,B,A)$ is shown as equation (2.1-1),

$$f(D,C,B,A) = A \cdot \bar{B} + B \cdot (C+D) \quad (2.1-1)$$

2.1 DECODER IMPLEMENTATION OF THE SUM OF MINTERMS CANONICAL FORM

2.1.1 Prepare a truth table of the given function f and of its complement \bar{f} , and show them as Table T2.1-1.

Hint#1 To avoid unnecessary loss of time while completing some later parts of the assignment, remember that the designation $f(D,C,B,A)$ implies that the list of variables in the truth table of the function is in the order D,C,B,A.

2.1.2 Using the truth table T2.1-1, prepare the decimal-list representations of both canonical forms (the sum of minterms and the product of maxterms) of the given function f and of its complement \bar{f} , and show them as equations (2.1-2) through (2.1-5) respectively.

2.1.3 Based on one of the algebraic representations (2.1-2) through (2.1-5), design a logic circuit which implements the function f using a 4 to 16 decoder circuit, which has active-high outputs. Implement the logic gate which will "sum" minterms as a degenerate two level combinational logic circuit. Show a graphical representation of the designed logic circuit as Figure 2.1-1.



Hint#2 Consider using the NOR-NAND, or NOR-AND *degenerate* two-level logic circuit (see lecture notes).

Hint#3 Note that the function f has ten minterms. Consequently, using the minterms of the complement of f will result in a simpler circuit for NOR-ing the minterms (and a higher grade).

2.1.4 Design a logic circuit which implements the function f using 3 to 8 decoder circuits available on a 74138 IC. Show a graphical representation of the designed logic circuit as Figure 2.1-2(a). Are Hint#2 and Hint#3 pertinent to the design of this circuit?

Hint#4 Note that 74138 IC has active-low outputs, and adjust the circuit correspondingly. Consider moving the bubbles from the outputs of the decoder to the inputs of the OR gate, and consider what impact that has on the function implemented by the gate. If you find that the OR gate is transformed into a NAND gate and that this does not implement the function f correctly, consider replacing the OR gate by an AND gate, and consider implementing that AND gate using a two-level NAND-NOR degenerate form. Check how the low-active outputs interact with the AND gate. Have a look at the list of available circuit components in Section 3.2.

Extra credit option: Study the Data Sheet information of the 74138 decoder IC, to find how one can avoid using inverters in supplying signals to the Enable inputs of the 74138 IC; then apply that connection to your version of the designed circuit.

2.1.5 Using integrated circuit components listed in section 3.2, design a physical layout of the logic circuit shown in Figure 2.1-2(a). Show a computer generated drawing of the designed layout as Figure 2.1-2(b). Provide IC package pinouts in all drawings of Figure 2.1-2.

Hint#5 Pinouts (pin numbers) are available in Figure 2.5 of the course text book, pp.107-109, and in the TTL Data Book.

2.2 MULTIPLEXER IMPLEMENTATION OF THE SUM OF MINTERMS CANONICAL FORM

2.2.1 Design a logic circuit which implements the function f using the 8:1 multiplexer available on the 74151A IC. Show the table that you applied in the design procedure as the Table 2.2-1.

2.2.2 Show a graphical representation of the designed logic circuit as Figure 2.2-1(a) (consult Section 4.4.3 of the course text book).

2.2.3 Using integrated circuit components listed in Section 3.2, design a physical layout of the logic circuit shown in Figure 2.2-1(a). Show a computer generated drawing of the designed layout as Figure 2.2-1(b). Provide IC package pinouts in all drawings of Figure 2.2-1.

Hint#6 Pinouts (pin numbers) are available in Figure 2.5 of the course text book, pp.107-109, and in the TTL Data Book.



3. Lab Equipment and Circuit Components

3.1 EQUIPMENT

Equipment to be used includes:

- Proto boards: Global PB-104, or PB-105,
- Agilent E3631A DC power supply,
- Function generator: Agilent 33120A,
- Mixed-Signal oscilloscope Agilent 54645D,
- Dell GxaEM computer system.

3.2 CIRCUIT COMPONENTS

- integrated circuit 7402, quad 2-input NOR gates (1)
- integrated circuit 7404, hex inverters (1)
- integrated circuit 7410, triple 3-input NAND gates (1)
- integrated circuit 7493, 4-bit ripple counter (1)
- integrated circuit 74138, 8:3 decoder (2)
- integrated circuit 74151A, 8:1 MUX (1)

4. Lab Experiment

4.1 DECODER IMPLEMENTATION

4.1.1 Using as a reference the drawing of the physical layout from Figure 2.1-2(b), build on the proto board the physical circuit that implements the function f . To test the circuit, add to the protoboard the auxiliary generator of all combinations of the four variables, A, B, C, and D. Figure A-4.1 shows the complete test circuit in which a pulse source (the function generator) and a binary counter serve as the generator of all combinations of the input variables.

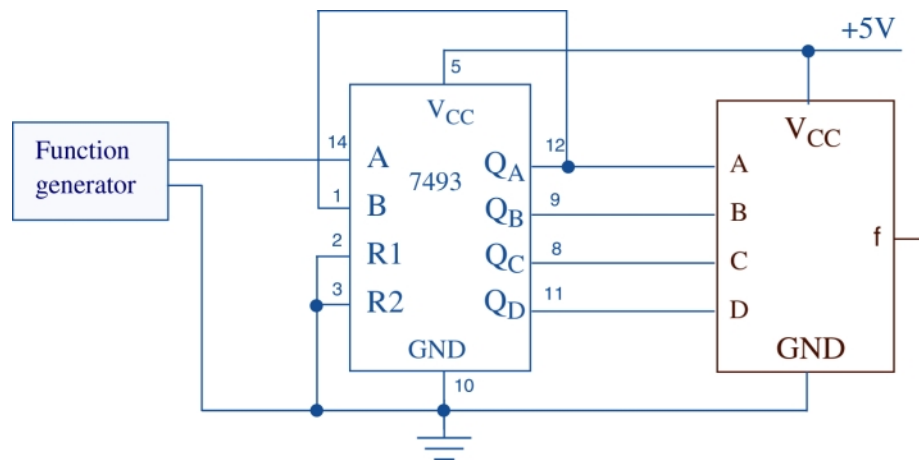


Figure A-4.1 The circuit for testing the implementations of function f .



4.1.2 Connect digital channels D0 through D4 of the Mixed-Signal oscilloscope Agilent 54645D to the circuit constructed under 4.1.1:

- digital channel D0: to the input A of the circuit which implements the function f ,
- digital channel D1: to the input B of the circuit which implements the function f ,
- digital channel D2: to the input C of the circuit which implements the function f ,
- digital channel D3: to the input D of the circuit which implements the function f ,
- digital channel D4: to the output f of the circuit which implements the function f .

Establish a ground connection. Turn on digital channels D0 through D4, and rename the channels D0 through D4 as A,B,C,D, and F respectively.

4.1.3 Adjust the frequency of the Agilent 33120A function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 0000 on channels D0 through D3. Hit the key Single on the Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 0000 on channels D0 through D3 is positioned at the left end of the screen, and that the whole screen shows ten percent more than two periods of the signal at input D.

4.1.4 Verify the correct functioning of the decoder circuit implementation of the function f by comparing the obtained waveforms to the truth table T2.1-1. If the waveforms do not match contents of the truth table, find and correct the error(s).

4.1.5 Save the Screen Image of the correct waveforms of the channels D0 through D5 to a file named L7_415.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.2 MULTIPLEXER IMPLEMENTATION

4.2.1 Using as a reference the prepared physical circuit diagram of Figure 2.2-1(b), build on the proto board the logic circuit which implements the function f using the 8:1 multiplexer component. To test the circuit which implements the function f , apply again the circuit shown in Figure A-4.1.

4.2.2 Apply the directives of sections 4.1.2 and 4.1.3 to the circuit constructed under 4.2.1.

4.2.3 Verify the correct functioning of the multiplexer circuit implementation of the function f by comparing the obtained waveforms to the truth table T2.1-1. If the waveforms do not match the contents of the truth table, find and correct the error(s).

4.2.4 Save the Screen Image of the correct waveforms of channels D0 through D5 to a file named L7_424.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.3 TRANSFER OF CAPTURED WAVEFORMS.

Transfer (ftp) the files L7_*.tif from the Dell GxaEM computer system to your personal College of Engineering computer account.



5. Postlab Assignment

As a part of the discussion of the design process, prepare a short analysis of topics listed below. Based on the design procedures applied in Sections 2.1.3 and 2.1.4 compare the circuit design considerations regarding the active-low and active-high IC output options.

6. Lab Report

To be considered complete, the lab report must contain the following,

1. Cover sheet - Lab style, filled out,
2. The truth table T2.1-1 prepared under 2.1.
3. The logic function expressions (2.1-2) through (2.1-5).
4. The design table T2.2-1 used in section 2.2.
5. The logic and physical circuit diagrams prepared as specified in Section 2.1 and 2.2.
6. The waveforms obtained under the conditions of Sections 4.1 and 4.2.
7. A report on items not already included under 1. through 6. above, which includes:
 - a discussion of the insights gained through the conducted experiments,
 - textual description and graphical/ tabular illustration of the design procedure(s),
 - description of implemented testing procedures,
 - conclusions reached as a result of performing the lab experiment,
 - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.